Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 22, 34, 37 and 38 as follows:

Listing of Claims:

1.-21. (Canceled)

22. (Currently Amended) An electronic device comprising:

a semiconductor chip;

an I/O pin on the semiconductor chip, for transmitting signals to a signal line outside of the semiconductor chip;

a transmitting circuit that is configured to selectively multiplex the plurality of signal lines onto the I/O pin; and

an initialization circuit, coupled to the transmitting circuit that selectively configures the transmitting circuit to multiplex at least one of the plurality of signal lines according to selection information and to transmit the selection information through the I/O pin, which is also used for subsequent data transmission.

23. (Previously Presented) The device of claim 22, further comprising a receiving circuit that is configured to receive multiplexed data from the I/O pin, and to reverse the multiplexing so that values originally from the multiplexed signal lines are separated into distinct signals in the receiving circuit.

24. (Previously Presented) The device of claim 23, wherein the transmitting circuit and the receiving circuit are driven by a common clock signal coupled to both the transmitting circuit and the receiving circuit.

25. (Previously Presented) The device of claim 23, further comprising a synchronizing circuit, coupled to the transmitting circuit, the synchronizing circuit sending a reset signal to the transmitting circuit, the transmitting circuit operable to transmit the selection information from the I/O pin upon receiving the reset signal and to subsequently send output signals from the I/O pin, the output signals multiplexed according to the selection information.

26. (Previously Presented) The device of claim 25, wherein the receiving circuit is coupled to the synchronizing circuit and operable to receive the reset signal, the receiving circuit receiving the selection information following receiving the reset signal and subsequently de-multiplexing the multiplexed signals according to the selection information.

27. (Previously Presented) The device of claim 25, wherein the initialization information is a signal line identifier.

28. (Previously Presented) The device of claim 23, wherein the transmitting circuit is located on the semiconductor chip and the receiving circuit is located off of the semiconductor chip.

29. (Previously Presented) The device of claim 23, wherein the receiving circuit is located on the semiconductor chip and the transmitting circuit is located off of the semiconductor chip.

30. (Previously Presented) The device of claim 22, wherein the semiconductor chip is a core logic chip that couples together a processor, a memory, and a peripheral bus in a computer system.

31. (Previously Presented) The device of claim 22, wherein the initialization circuit is located externally to the semiconductor chip.

32. (Previously Presented) The device of claim 22, wherein the initialization circuit is configured to initialize the transmitting circuit during a computer system boot up operation.

33. (Previously Presented) The device of claim 22, wherein the transmitting circuit includes: a multiplexer for multiplexing the plurality of signal lines onto the I/O pin; and a control circuit that controls the multiplexer so that the at least one of the plurality of signal lines is multiplexed onto the I/O pin.

34. (Currently Amended) An electronic device comprising:

an I/O pin; and

a semiconductor chip coupled to the I/O pin and comprising a receiving circuit that is configured to selectively de-multiplex signals from the I/O pin onto a plurality of internal signal lines, the receiving circuit having a reset line and being configured to receive configuration data through the I/O pin upon receiving a signal on the reset line and to thereafter de-multiplex signals from the I/O pin according to the configuration data.

35. (Previously Presented) The electronic device of claim 34, wherein the semiconductor chip is a first semiconductor chip, the device further comprising a second semiconductor chip coupled to the I/O pin and the reset line and including a transmitter, the transmitter operable to transmit configuration data from the I/O pin upon receiving a signal on the reset line and to subsequently send multiplexed signals from the I/O pin according to the configuration data.

36. (Previously Presented) The electronic device of claim 34, wherein the configuration data is one or more signal line identifiers each corresponding to one of the plurality of signal lines.

37. (Currently Amended) The electronic device of claim 34, wherein the transmitting circuit and the receiving circuit are driven by a common clock signal coupled to both the transmitting circuit and the receiving circuit.

38. (Currently Amended) The ~~apparatus~~electronic device of claim 34, wherein the reset signal is sent to the transmitting circuit and the receiving circuit during a computer system boot up operation.

39. (Previously Presented) A method for multiplexing signals comprising:

exerting a reset signal on a semiconductor chip having a transmitter circuit and an initialization circuit, the initialization circuit receiving the reset signal and causing the transmitter to serially transmit configuration information on a single I/O pin;

transmitting data signals to the transmitter over a plurality of signal lines coupled to the transmitter; and

the transmitter multiplexing the data signals from selected lines of the plurality of signal lines on the I/O pin, the selected lines being identified by the configuration information.

40. (Previously Presented) The method of claim 39, wherein the semiconductor chip is a first semiconductor chip, the method further comprising receiving the configuration data at a second semiconductor chip including a receiving circuit, the receiving circuit de-multiplexing the data signals according to the configuration data.

41. (Previously Presented) The method of claim 39, further comprising waiting for a delay period after exerting the reset signal before causing the transmitter to serially transmit the configuration information.